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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,646	01/06/2006	Francesco Pessolano	NL030809	1901
65913 NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131	7550 04/30/2010		<div>EXAMINER</div> <div>PETRANEK, JACOB ANDREW</div>	
			<div>ART UNIT</div> <div>2183</div>	<div>PAPER NUMBER</div>
			<div>NOTIFICATION DATE</div> <div>04/30/2010</div>	<div>DELIVERY MODE</div> <div>ELECTRONIC</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/563,646

Applicant(s)

PESSOLANO, FRANCESCO

Examiner

Jacob Petranek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/4/2010.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-20 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/CD)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-20 are pending.
2. The office acknowledges the following papers:
Claims and arguments filed on 3/4/2010.

Withdrawn objections and rejections

3. The drawing objection for claim 7 has been withdrawn.

Maintained Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-6, 8-9, and 11-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wilkerson et al. (U.S. 7,143,272).
6. As per claim 1:
Wilkerson disclosed an apparatus for predicting a conditional branch outcome within a computer system, the apparatus comprising
an activity monitor, responsive to identifying an occurrence of a conditional branch (Wilkerson: Figures 4 and 6 elements 225 and 605, column 4 lines 32-45 and column 5 lines 62-67 continued to column 6 lines 1-15)(The computation history generator is the activity monitor that monitors all information that affects the current

instruction. It's obvious to one of ordinary skill in the art that the computation history generator is aware of branch instructions because the index calculator is used for branch instructions instead of the computation history generator.), the activity monitor providing a measure of system activity, indicative of a level of logic state changes, since a previous branch for comparison with data relating to previous system activity (Wilkerson: Figures 4 and 6 elements 225, 230, and 320-5, column 4 lines 32-45 and column 5 lines 19-28 and lines 52-61)(The hashing of the computation history allows each computation history to identify all values that affect the current value of the register. Computation histories are an instance of a data flow graph, which identifies how much activity has occurred to assist in making a branch prediction. Therefore, the computation history can be indicative of how many logic state changes have occurred by how much activity has occurred for the specific register. Official notice is given that lookup tables can be arranged to have tags for insuring that the index does retrieve the correct data. Thus, it's obvious to one of ordinary skill in the art that element 230 contains a tag that is used to compare with the activity since a previous branch), the conditional branch outcome being predicted based on such comparison (Wilkerson: Figure 9 element 925, column 6 lines 16-22)(The branch prediction is retrieved from the lookup table upon a hit in the lookup table.).

7. As per claim 2:

Wilkerson disclosed the apparatus according to claim 1, wherein the data relating to system activity comprises average system activity (Wilkerson: Figure 4 element 225,

column 5 lines 19-28)(The computation history is a running average of previous computation histories.).

8. As per claim 3:

Wilkerson disclosed the apparatus according to claim 1, wherein an activity history table is provided that stores and associates previous system activity with corresponding outcomes of previous branches (Wilkerson: Figure 6 element 230, column 6 lines 16-22)(The lookup table stores branch predictions based on previous predictions.).

9. As per claim 4:

Wilkerson disclosed the apparatus according to claim 3, wherein data relating the system activity between the conditional branch and the previous branches is retrieved for comparison with the data contained in the activity history table (Wilkerson: Figures 6 and 9 elements 230 and 915, column 5 lines 19-28 and column 6 lines 16-22 and lines 59-66)(The lookup table is accessed for comparison purposes to find a match between the index and a stored prediction.), the conditional branch outcome being predicted based on selecting the previous branch outcome associated with activity history data which most closely resembles the retrieved system activity data (Wilkerson: Figure 9 element 925, column 6 lines 16-22)(The branch prediction is retrieved from the lookup table upon a hit in the lookup table. The hit indicated previous activity that most closely resembles current activity.).

10. As per claim 5:

Wilkerson disclosed the apparatus according to claim 4, wherein the activity history table is updated based on activity data associated with the conditional branch outcome (Wilkerson: Figure 9 element 930, column 7 lines 4-6)(The lookup table is updated based on the branch outcome.).

11. As per claim 6:

Wilkerson disclosed the apparatus according to claim 1, wherein the conditional branch outcome is predicted using the outcome history of the conditional branch (Wilkerson: Figure 9 element 925, column 6 lines 16-22)(The branch prediction is retrieved from the lookup table upon a hit in the lookup table and is used to predict the outcome of the current branch instruction.).

12. As per claim 8:

The additional limitation(s) of claim 8 basically recite the additional limitation(s) of claim 1. Therefore, claim 8 is rejected for the same reason(s) as claim 1.

13. As per claim 9:

The additional limitation(s) of claim 9 basically recite the additional limitation(s) of claim 2. Therefore, claim 9 is rejected for the same reason(s) as claim 2.

14. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 3. Therefore, claim 11 is rejected for the same reason(s) as claim 3.

15. As per claim 12:

The additional limitation(s) of claim 12 basically recite the additional limitation(s) of claim 4. Therefore, claim 12 is rejected for the same reason(s) as claim 4.

16. As per claim 13:

The additional limitation(s) of claim 13 basically recite the additional limitation(s) of claim 5. Therefore, claim 13 is rejected for the same reason(s) as claim 5.

17. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 6. Therefore, claim 14 is rejected for the same reason(s) as claim 6.

18. Claims 7 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wilkerson et al. (U.S. 7,143,272), in view of Chang et al. ("Improving branch prediction accuracy by reducing pattern history table interference").

19. As per claim 7:

Wilkerson disclosed the apparatus according to claim 6.

Wilkerson failed to teach wherein data relating to the activity of the system is only used for branch outcome prediction if the confidence of accuracy of branch outcome prediction using branch history is relatively low.

However, Chang disclosed wherein data relating to the activity of the system is only used for branch outcome prediction if the confidence of accuracy of branch outcome prediction using branch history is relatively low (Chang: Figure 5, section 4.1)(The combination results in the prediction system of Wilkerson being used by default and the BTB high confidence predictor of Chang being used to predict high-confidence branches.).

The advantage of using the two structure predictor of Chang is that it allows for reducing interference from branch history tables, which can also improve branch prediction performance (Chang: Section 4.1 paragraph 1). One of ordinary skill in the art would have been motivated by this advantage to implement the two-structure predictor of Chang into Wilkerson. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two-structure predictor of Chang into the processor of Wilkerson for the advantage of reducing interference in the lookup table and increasing branch prediction performance.

20. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 7. Therefore, claim 15 is rejected for the same reason(s) as claim 7.

21. Claims 10 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wilkerson et al. (U.S. 7,143,272), in view of LeFevre et al. (U.S. 6,854,066).

22. As per claim 10:

The additional limitation(s) of claim 10 basically recite the additional limitation(s) of claim 16. Therefore, claim 10 is rejected for the same reason(s) as claim 16.

23. As per claim 16:

Wilkerson disclosed an apparatus according to claim 1.

Wilkerson failed to teach wherein the activity monitor monitors supply current.

However, LeFevre disclosed wherein the activity monitor monitors supply current (LeFevre: Column 2 lines 51-67 continued to column 3 lines 1-15)(LeFevre disclosed a

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power management system to monitor current usage. It's obvious to one of ordinary skill in the art that the power management system and the branch predictor of Wilkerson can be performed in the same unit. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

The LeFevre power management system has the advantage of monitoring power consumption without being reconfigured for adding and removing system components (LeFevre: Column 2 line 67 continued to column 3 lines 1-6). One of ordinary skill in the art would have been motivated by this advantage to implement the power management system into the processor of Wilkerson. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the power management system of LeFevre into Wilkerson for the advantage of monitoring power consumption without reconfiguration for portable systems.

24. Claims 17-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wilkerson et al. (U.S. 7,143,272), in view of Kime et al. ("Logic and computer design fundamentals").

25. As per claim 17:

Wilkerson disclosed an apparatus according to claim 1.

Wilkerson failed to teach wherein the activity monitor includes a series of logic elements including a plurality of sequential logic elements clocked by a clock signal and plurality of combinatorial logic elements connecting the sequential logic elements such

that, for a given clock signal cycle, counting state changes within the logic elements provides the measure of system activity.

However, Kime disclosed wherein the activity monitor includes a series of logic elements including a plurality of sequential logic elements clocked by a clock signal (Kime: Section 5-3)(Wilkerson: Figure 4 element 430)(The shifting logic is shown in more detail by Kime by having sequential logic as the building blocks of a shifter.) and plurality of combinatorial logic elements connecting the sequential logic elements (Kime: Figure 3-3, sections 3-1 and 3-2)(Wilkerson: Figure 4 element 425)(The XOR logic is shown in more detail by Kime by having sequential logic as the building block of the XOR element.) such that, for a given clock signal cycle, counting state changes within the logic elements provides the measure of system activity (Wilkerson: Figure 4 element 410)(A state change occurs for the computational history each time an instruction is executed.).

Wilkerson disclosed higher-level logic elements, but failed to detail the individual lower-level combinational and sequential logic circuits that make up the higher-level circuits. One of ordinary skill in the art would have been motivated by this lack of information to find Kime that discusses the lower-level details of how combinational and sequential circuits are build from the ground up. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the lower-level circuits of Kime into the higher-level circuits of Wilkerson to show in detail how the circuits of Wilkerson are build and designed.

26. As per claim 18:

Wilkerson and Kime disclosed an apparatus according to claim 17, wherein the sequential logic elements include flip-flops (Kime: Section 5-3).

27. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claim 18. Therefore, claim 19 is rejected for the same reason(s) as claim 18.

28. As per claim 20:

Wilkerson and Kime disclosed an apparatus according to claim 17, wherein the combinatorial logic elements include processing logic blocks and data path logic blocks (Kime: Figure 3-3, sections 3-1 and 3-2).

Response to Arguments

29. The arguments presented by Applicant in the response, received on 3/4/2010 are not considered persuasive.

30. Applicant argues "In making this assertion the Office Action at page 4 argues that "computation history can be indicative of how many logic state changes have occurred by how much activity has occurred for the specific register." The Office Action cites to no portion of the '272 reference to support this assertion, and it appears to Applicant that there is no support for such an assertion in the '272 reference. Moreover, given a multitude of different types of computation and/or compilations thereof, Applicant fails to appreciate the logic behind this unsupported conclusion. Therefore, the '272 reference, alone or in combination with any of the asserted references, fails to provide correspondence to the claimed invention."

This argument is not found to be persuasive for the following reason. Wilkerson disclosed in column 5 lines 19-28 and lines 52-61 that computation histories are recursively computed and is essentially a trace of the "entire genesis of the current data value in the register" that is to be used for branch prediction. Additionally, Wilkerson disclosed that the computation history can also be thought of as a data flow graph. One of ordinary skill in the art would clearly recognize that a data flow graph provides an indication of the level of logic state changes since a previous branch, as well as the computation history value itself being continuously modified and shifted upon each use of the register can give an indication of the level of logic state changes since a previous branch. Thus, the computation history values being continuously modified reads upon the claimed limitation.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jacob Petranek/
Examiner, Art Unit 2183

